CHAPTER FOUR

INPUT/OUTPUT CONTROL ELEMENT

4-1. INTRODUCTION

The IBM 7231-02 Input/Output Control Element provides the linkage between the Input/Output devices and the 9020 System. The IOCE provides communication between the I/O devices and the SE as specified by instructions from the CE. A simplified IOCE data flow is shown on Fig. 4-1. Note that the IOCE primarily interfaces with other elements in the system. The channels noted on the diagram include 2, (or possible 3), Selector Channels and 1 Multiplexor Channel. These channels act as the interface between the various I/O devices and the IOCE. The IOCE has many functional units in common with the CE; however, due to different operational requirements it also contains some unique functional units. The IOCE has 8,192 (32K (20K hex)) words of storage referred to as MACH Store. Of these 1,024 (1 BUMP STORE) are used for channel control words associated with the Multiplexor Channel. ROS within the IOCE makes use of two modes of operation. One mode, CPU mode, operates identically with the Compute Element in processing instructions. The second mode is unique to the IOCE and is referred to as I/O mode. In I/O mode the various channel functions are performed on a priority basis. I/O mode overrides CPU mode and permits channel operations to take precedence over CPU functions. The IOCE utilizes Local Store to a greater degree than does the CE since all channel operations are dependent upon local store control words for their operation.

Before going into any detailed discussion on the functional units of the IOCE, we should become acquainted with the differences between the Selector and Multiplexor Channels. Also we must define some of the more commonly used terms. As both the IOCE and the CE have the same functional units in the area referred to as the Common Logic Unit (CLU), discussion will be limited to those function units which are unique to the IOCE. Reference should be made to the CE sections whenever a question arises about the units which are common to both.

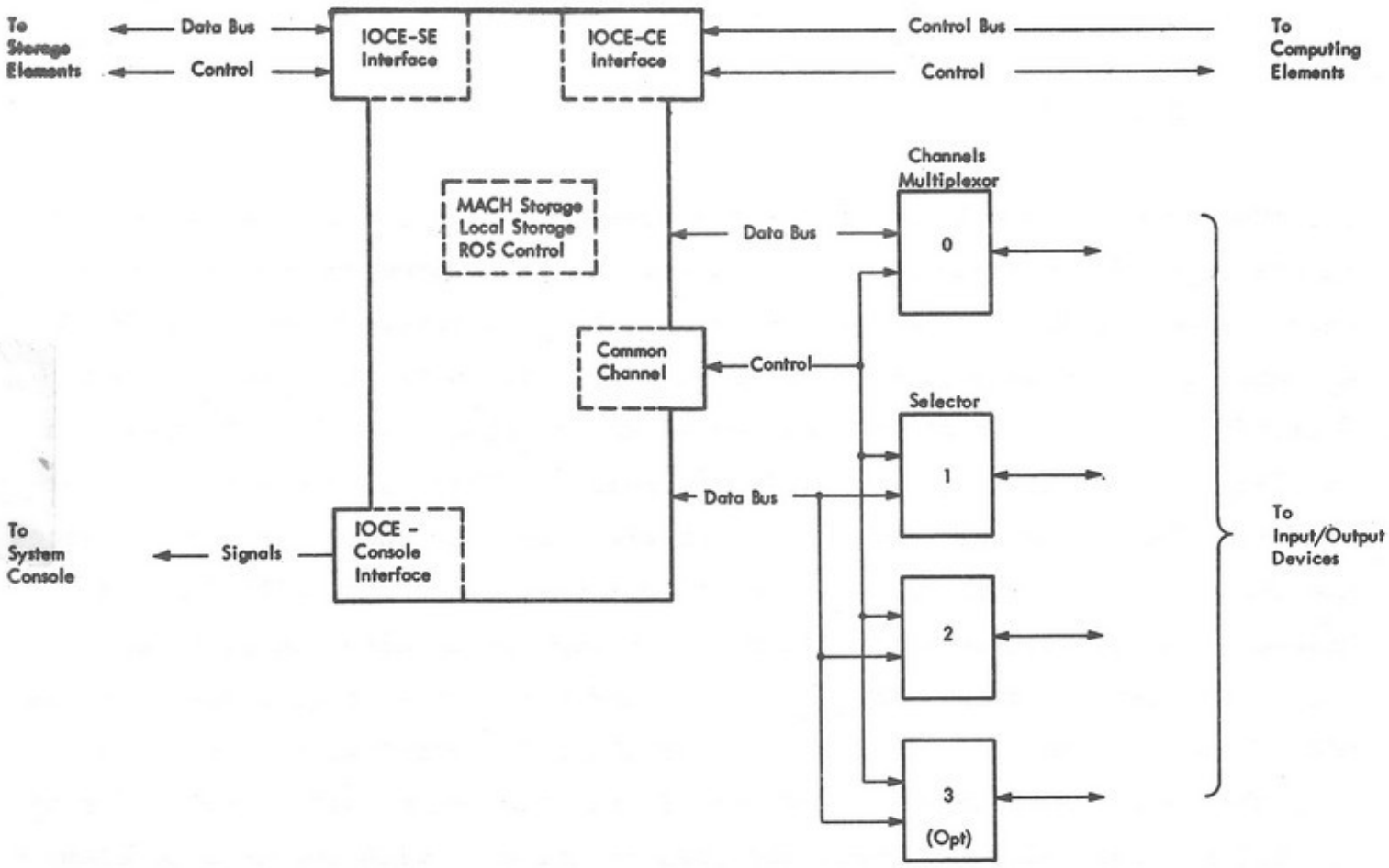


Figure 4-1. Simplified IOCE Data Flow.

The Multiplexor Channel is capable of servicing several I/O devices on a byte interleave basis simultaneously in multiplex mode or a single device at a time when operating in burst mode. The Multiplexor Channel uses the CLU only for the length of time required to service the I/O device request and requires fetching control words for each device from MACH Store when the channel is operating in multiplex mode. When in "burst" mode, the Multiplexor Channel can only service one device at a time and the channel retains control of the CLU for the entire duration of the operation. The Multiplexor utilizes special I/O mode ROS routines in its operation and utilizes the CLU extensively for its data transfers.

The Selector Channel on the other hand may operate only in burst mode, and as such may control only one device at a time. The control words being used by the Selector Channel during an I/O operation are stored in Local Store and

are more rapidly available to the IOCE for use. (MACH Store cycle time = 2 μsec, Local Store cycle time = 0.5 μsec.) Then too, since only one device is being serviced at any given time, the control words need not be fetched and re-fetched. The Selector Channels use conventional sequential logic circuits to control operations and require the use of the microprogram and CLU only when data transfers are to be accomplished between the IOCE and the Storage Element. (Using the data supplied by the Program I/O Instruction, the channel assigns priority to these ROS routines and requests them as needed.)

Another factor which tends to speed up operations on the Selector Channels is the fact that data is handled on a full word basis whereas on the Multiplexor Channel the data is handled on a byte basis.

4-2. PHYSICAL MAKE-UP

The IOCE like the CE utilizes the same "building block" construction techniques. It is made up of the same card, board, gate and frame arrangement as the previously discussed Compute Element; however, in the case of the IOCE there are some additions. Frame 01 contains the logics for the CLU and the channels. Frame 02 contains the logics and the core array for the MACH storage. Frame 03 contains the power supplies, the configuration control circuitry, and the optional 3rd channel.

4-3. UNIQUE IOCE FUNCTIONAL UNITS FOR SELECTOR CHANNEL

Figure 4-15 is the overall data flow diagram for the IOCE. From this it may be seen that with the exception of the I/O oriented registers, the basic CLU is identical with that of the CE. The I/O oriented functional units for Selector Channel will be briefly discussed in the following sections.

A. B Register

The B Register acts as a buffer to data being transferred to or from the C Register. All data enroute to or from channel passes through this register. While the logic diagrams (ALDs) and the data flow chart indicate only one B Register, there is actually one of these register per Selector Channel. ALD representation for these registers is ALWAYS WITH REFERENCE TO SELECTOR CHANNEL NUMBER ONE....To determine the card location for Selector Channel 2, take the board card location from the ALDs and subtract 2 from the board location, e.g. a bit position for the B Register is given as E gate, board D4 card F6. The equivalent bit position for Selector Channel 2 B Register is E gate, board D2 card F6. To determine the card location for the optional 3rd channel, the J gate is substituted for the specified E gate location on the ALDs.

B. C Register

The C Register is used for distributing the word from storage to the channel on a byte basis. This register is also used to assemble the incoming bytes from channel into a word prior to sending it to storage. Like the B Register, there is one C Register per Selector Channel. The C Register is fed directly from the channel interface on input operations and placed its output into the B Register. On output operations the C Register is fed from the B Register and places its output directly on the channel interface bus. The rules for finding card locations for channel 2 and 3 are the same as for the B Register. Figure 4-2 should be examined for relative board locations.

Since both the ~~C~~ B and C Registers are concerned with the operations in the Selector Channel, it may be wise at this time to cover the remainder of the registers whose application is primarily in this area. This is the area enclosed by the dashed line in Fig. 4-15. The logical units are also shown in greater detail in Fig. 4-16. In this figure they are related to the CLU functional units with which they operate. For convenience and ease in correlating these diagrams to the ALDs, the corresponding ALD pages are

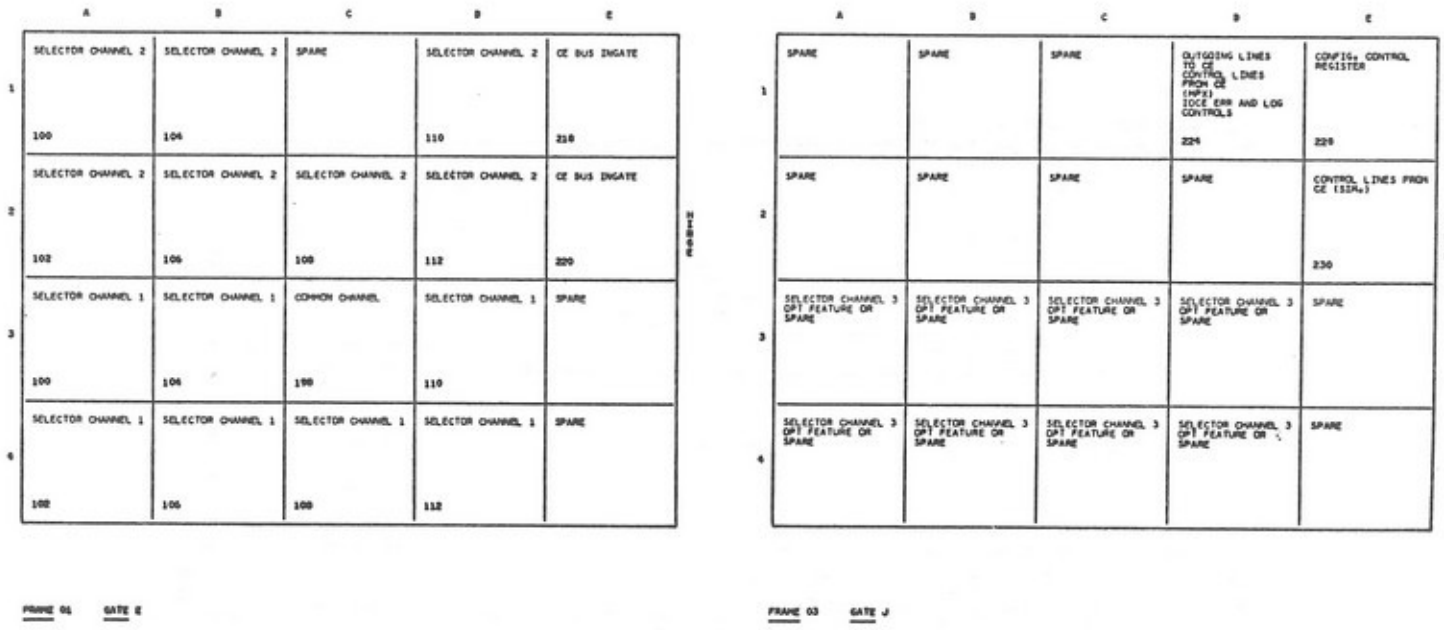


Figure 4-2. Selector Channel Board Locations.

included. In Selector Channel operation the hardware circuits make use of the programmer supplied control words such as the Command Address Word (CAW) and the Channel Command Word (CCW). Since only one control unit may be operating on a channel at a time in the Selector Channel, the information is stored in the General Purpose Register. It is from this register then that the Selector Channel derives operational control. Because the General Purpose Register can store only eleven bits, the outputs of several register positions have more than one destination. These positions are modified with appropriate data more than once while the channel is processing the CCWs.

C. General Purpose Register

Figure 4-4 shows the contents of the General Purpose Register for various channel states. The logic flow of Fig. 4-3 indicates that the General Purpose Register feeds the Byte Counter, the End Register, the Operation Register, and the Flag Register.

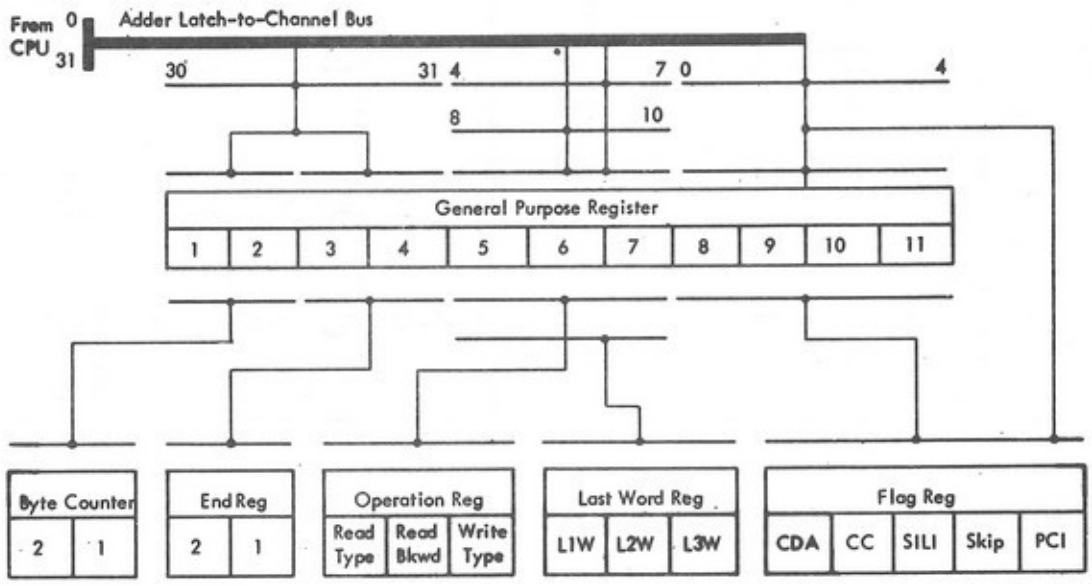


Figure 4-3. General Purpose Register Logic Flow.

General Purpose Latches							
1	2	3	4	5	6	7	Channel State
0	0	0	0	0	0	0	Idle → CCW-1, Step 1
← BC Information →		0	0	Rd Op	Bkwds	Wr Op	CCW-1, Step 1 → CCW-2, Step 1
← BC Information →		0	0	0	0	0	CCW-2, Step 1 → CCW-2, Step 2
← BC Information →		← ER Information →		L1W	L2W	L3W	CCW-2, Step 2 → CCW-2, Step 3 A1
← BC Information →		0	0	L1W	L2W	L3W	CCW-2, Step 3 A1 → Rd Store or Wr Fetch
← MBCR Information →				L1W	L2W	L3W	Rd Store
← BC Information (Original) →		0	0	L1W	L2W	L3W	Wr Fetch
—	—	← BC Information (Final) →		L1W or Compare Equal	L2W	L3W	End Up (Rd) → Interrupt → Reset
← BC Information (Original) →		0	0	L1W or Compare Equal	L2W	L3W	End Up (Wr) → Interrupt → Reset

Figure 4-4. General Purpose Register Utilization.

D. Byte Counter

Figure 4-3 indicates that the General Purpose Register positions 1 and 2 feed the Byte Counter. This Byte Counter is used to control byte selection within the C Register. The Byte Counter set to 00 selects byte 0 of the C Register, Byte Counter set to 01 selects byte 1 of the C Register and so forth through byte 3. The Byte Counter is made up of two stages of logic. The A side is used to select C Register byte positions and is stepped upon the completion of a data transfer across the interface. The B side of the Byte Counter is used to determine, early in the operation, if the the present data sequence with the interface will transfer the last byte to be stored (or fetched) from the designated storage block. It is also used to store or unload the byte in C Register byte 3. The B side of the counter is advanced when the interface data sequence begins. Figure 4-5 is a second level logic diagram of the Byte Counter and its gating circuitry.

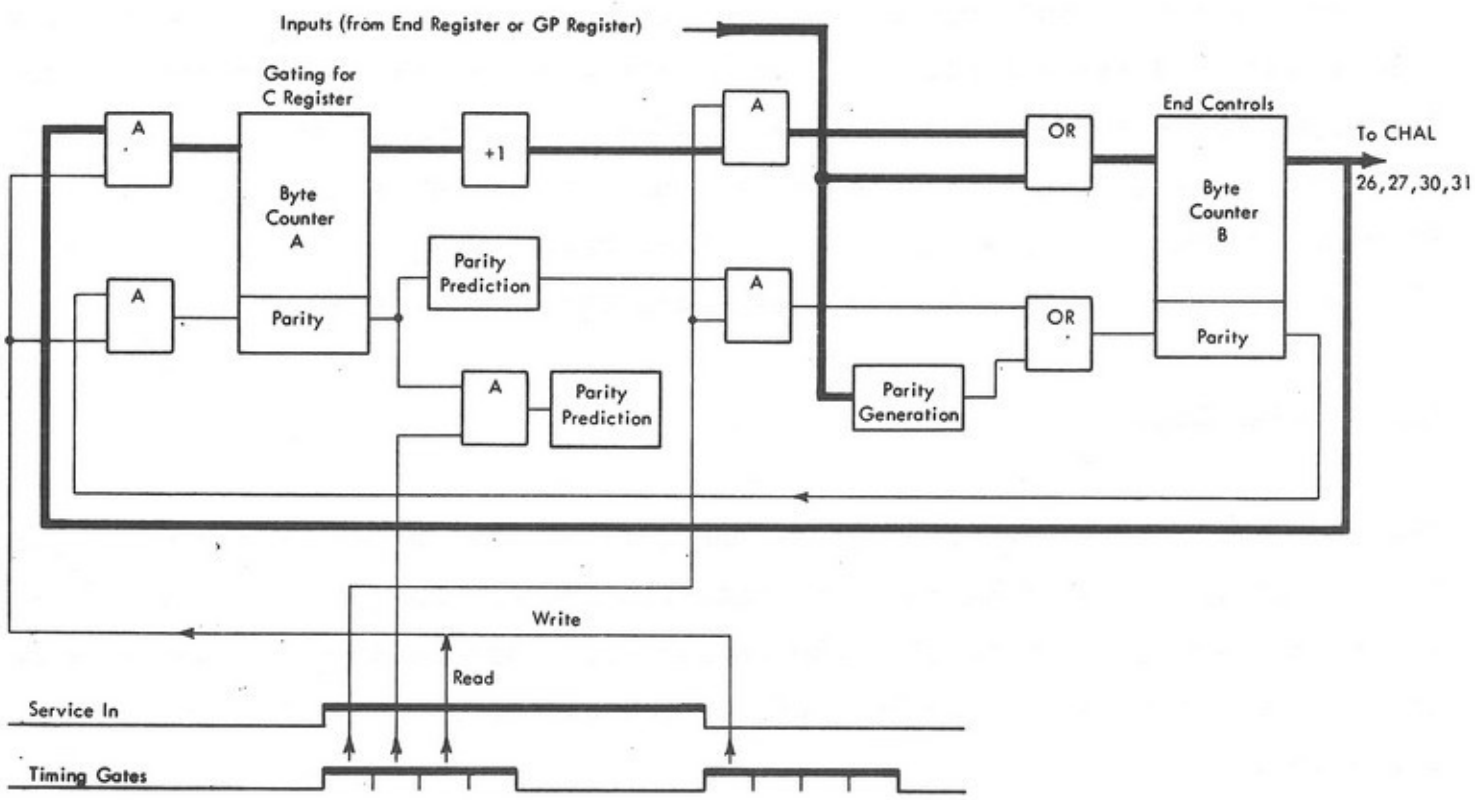


Figure 4-5. Channel Byte Counter.

E. End Register

Bits 3 and 4 of the General Purpose Register are used to contain the results of adding the last two bits of the data address with the last two bits of the count. The resultant is placed in the End Register for use when an off-bounds data transfer between the channel and storage exists.

F. Last Word Register and Operation Register

Bits 5, 6, and 7 of the General Purpose Register may contain either the last word information or the Operation Register information. In operation the CCW can specify one of five commands that may require communication between the channel and an I/O unit. The channel cannot distinguish between write and control or between sense and read command; therefore, the commands are divided into three categories: Read, Read Backward, and Write. The CLU transfers bits to the channel to identify a command. The channel decodes the bits and sets one of three positions of the Operation Register. The last word information takes on different significance in the Read and Write operations. In Read operations a Last Word Register position is normally set when three or less words are left to be stored in the designated block in main storage; whereas in the write operation a Last Word Register position is set after the last word is taken from the designated storage position.

G. Flag Register

The Flag Register is set from positions 8-11 of the General Purpose Register. The set state of any Flag Register position causes channel to deviate from normal procedures in executing the operation. This register is normally set while processing the second half of the CCW except in the write chain data operation.

H. Channel Status Register

The Channel Status Register is supplied with data from the common channel circuits. This data is used to indicate the following:

1. Program Controlled Interrupt
2. Incorrect Length Indication
3. Program Check
4. Protection Check
5. Channel Data Check
6. Channel Control Check
7. Interface Control Check
8. Chain Check

Any bit set in this register will appear as information in the Channel Status Word when a channel interrupt occurs, and may be utilized by the programmer to ascertain the ending status of the operation.

Referring once again to Fig. 4-15 the remaining functional units of the Selector Channel may be divided into two categories. The first of these is the priority and routine request circuitry, and the second is the external channel and interface controls.

I. Routine Request Circuitry, I/O External Channel, and Interface Controls

In the operation of the IOCE an area of circuitry called common channel deals with all circuitry common to the Multiplexor Channel and the Selector Channels. This circuitry processes requests for service from the channels, and assigns priorities to the service requirements. All requests are held active until they are serviced and the routine requested is in progress. The priorities assigned indicate that requests for Local Storage Read, and Local Store Write routines, carry the highest priority (referred to as higher than 1). The Write Fetch or Read Store routines are assigned as priority 1 since these routines imply that an I/O device is awaiting immediate data service and the

possibility of a channel over-run is impending. On the other hand Interrupt Preparation or instruction (SIO) processing are assigned the lowest priority (priority 3) since these in general are not time dependent (within limitations). Figure 4-6 is a second level logic diagram depicting the interrelationship between the Priority Circuits, the Request Register, and the Position Register in the Selector Channel operation.

4-4. CHANNEL ROS RELATIONS

Although channel can perform a limited number of actions without direction from the Read Only Storage, neither the multiplexor nor the selector can operate completely independent of this control. Since it is possible for the CLU to be performing operations other than the servicing of the channel requests when a request is received that requires the use of the functional units of the CLU, ROS is required to switch from the CPU mode of operation to I/O mode of operation. This is defined as Break-in and may be accomplished any time that the CLU is operating in the CPU mode and is not in the R-1 or R-2 cycle of the storage timing ring. Break-in always occurs at zero time of the machine cycle and results in the degating to the ROSDR (that is, all of the μ-orders are decoded as no-ops) and the R Register is automatically backed up into local store quadrant two, word twelve. The ROS address of the CPU mode instruction which was to have been processed at the time of the break-in is stored in the I/O Back-up Register for the subsequent breakout. (After the break-in cycle is completed and the ROS is operating in the I/O mode, the I/O Backup Register is not altered.) When operating in the I/O mode, the sequence of ROSDR bits, which go to make up a field, are altered and the method of decoding these fields is changed to permit additional μ-orders applicable only to this mode of operation.

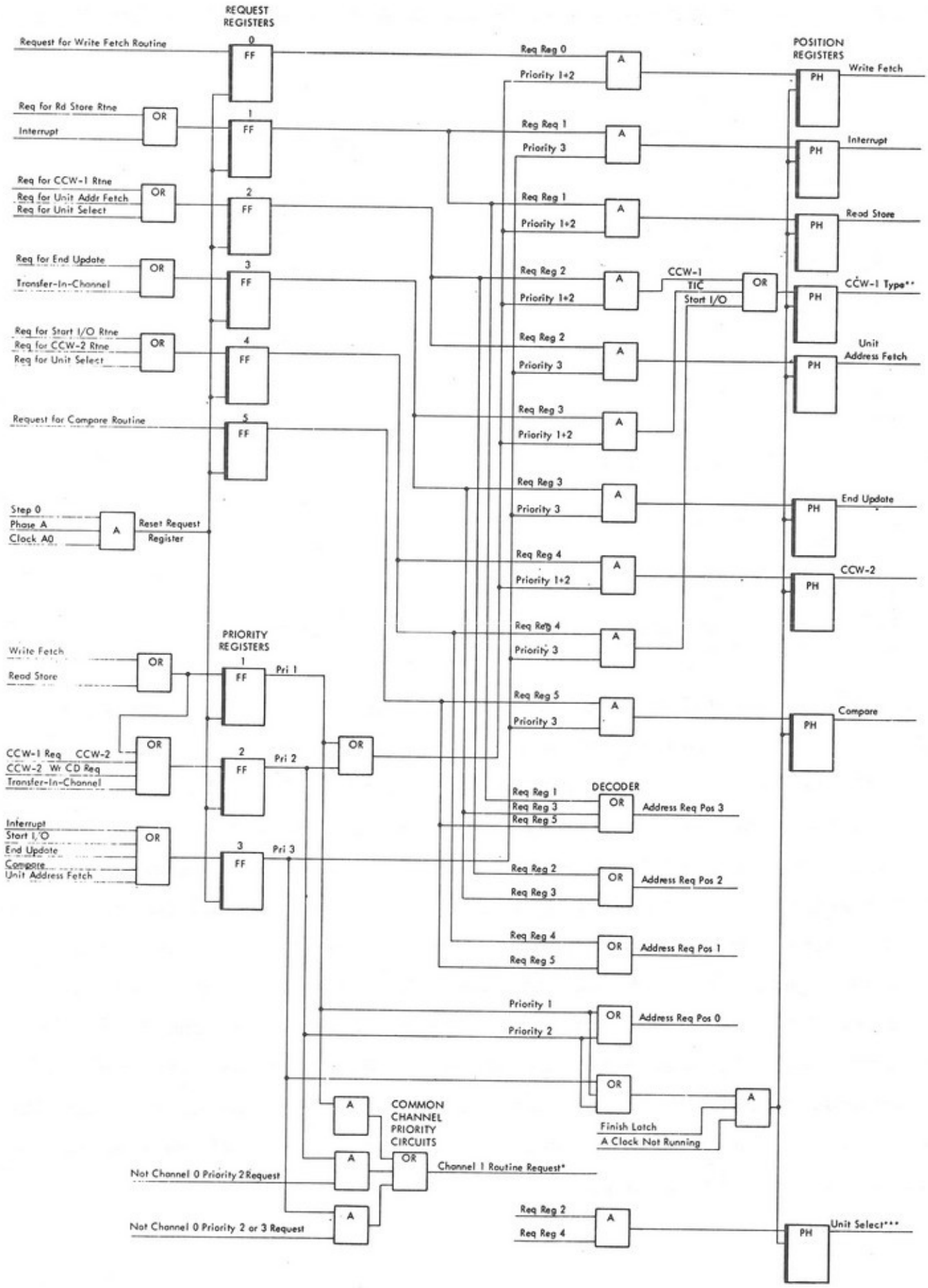


Figure 4-6. Routine Request and Priority Circuits.

There are twelve ROS routines used in the IOCE to service Selector Channel requirements. These are:

	Routine Name	ROS Address
1.	Start I/O	0010
2.	Transfer-in-Channel	002C
3.	CCW-1	0028
4.	CCW-2	0030
5.	Write Fetch	0020
6.	Read Store	0024
7.	Compare	0014
8.	Unit Address Fetch	0008
9.	End Update	000C
10.	Interrupt	0004
11.	Local Store Read	0040
12.	Local Store Write	0044
13	Set ATR	
14	Read Store routine	

Each of the aforementioned ROS routines performs a different service to the channel. For more complete details of these services, the student is advised to consult the CAS logic diagrams for the specific IOCE. The first ROS address of each of the routines is generated by the routine request circuitry. This circuitry consists of two registers. A six position register referred to as the Request Register, and a three position register called the Priority Register. These two sets of registers drive or set the position register as well as signal common channel to force the first ROS address of the requested routine. Since there are two Selector Channels in the IOCE, there are control registers for both, and while the ALD listings refer only to Selector Channel number one, the appropriate Selector Channel two circuits may be determined as previously mentioned. The optional channel three circuitry may also be found on gate J.

4-5. CE - IOCE SELECTOR CHANNEL OPERATION

Examination of a Start I/O instruction to a specific device on the Selector Channel shows that the instruction is fetched from storage by the CE and the initial data movements are accomplished to gate proper data to the CE's External Register. The flowcharts (Figs. 4-17 and 4-18) in conjunction with the Data Flow Diagrams (Figs. 2-64 and 4-15) for the CE and IOCE may be examined to clarify the locations and paths within the CE and IOCE. Notice from the flowcharts that once the CE has sent the I/O Op Signal to the IOCE that it (the CE) goes into a countdown loop to await a response from the IOCE. The data to be used in this instruction would be stored at the following storage locations prior to execution of the SIO.

Storage Location	Date	Comments
0A00	9C000101	Start I/O to Tape Drive
0048	0000A000	Channel Address Word (CAW) specifying a key of zero' and a command address of A000
A000	0200C000	Channel Command Word-1 (CCW-1) with a read command and a data address of C000
A004	20000020	Channel Command Word-2 specifying a SILI flag set on and a byte count of X'20' bytes

For proper operation of the instruction it must be assumed that the current PSW is properly masked to allow the execution of this privileged instruction and that the Selector Channel is properly masked to allow the subsequent I/O interrupt. Bear in mind that the PSW under consideration is contained in the CE only. Any channel masking will be taken care of via intercommunication linkage. We are also concerned with two ROS control units. The ROS of the CE will be concerned with the instruction fetching and initial processing. The IOCE ROS on the other hand will operate as follows:

The IOCE ROS unit is normally operating in CPU mode. When this element is not processing I/O instructions, processing interrupts, performing logouts, or performing other maintenance functions, ROS is cycling in the halt or wait loop. (The IOCE must be in the wait loop before any processing of this instruction can take place.) Under the conditions mentioned, a General Purpose Stat (stat 1) is set and branching from the halt loop will take place under its influence. The IOCE will permit its circuits to gate the data from the CE external register into its own functional units. Under the control of the I/O op code sent from the CE, the IOCE will branch to the appropriate μ-routine to handle the requested operation. In the case of the SIO, this would require the fetching of the CAW from the SE and using the address contained in this word to fetch CCW-1. When if the CCW is tested and found to be valid, the IOCE will take the data it has available from the CE external register, the CAW, and CCW-1, and gate it to the correct functional registers. When this is completed, the IOCE raises a tag line to the Common Channel, then establishes and enters its own count'down loop. The tag line to the Common Channel in our case causes Common Channel to force the first address of the Selector Channel SIO ROS routine. As a result of forcing the ROS address and the ensuing break-in, the IOCE goes to I/O mode. (Until this time the IOCE has been operating in CPU mode.)

As was mentioned previously, in the I/O Mode, the IOCE ROS routines are used to perform the functions or services as requested by the Selector Channel's logic circuits. In a read operation for instance, channel data is accepted by the IOCE circuits and routed to the appropriate storage facilities under ROS routine and channel logic circuit control. The ROS routine synchronizes the Channel Clock to start taking data off the bus with a DTC pulse on the cycle prior to its putting data on the bus. The data may be Unit Address, Data Address, or Chaining Flags (I/O data during Write operations also).

The SIO ROS routine places the Unit Address in C Register byte 0 and the Operation Code in the B Register byte 0. It also sets the Byte Counter and places the Command Address, Data Address, and Unit Address in Local Store. A test is made for a Transfer-In-Channel (TIC) command, and a request is made

of Common Channel for CCW-2 routine. Assuming the request for CCW-2 will be honored immediately, there will be no break out cycle at this time.

The CCW-2 routine fetches the CCW-2 word from storage and stores the bits for the Flag, End, and Last Word Registers in the General Purpose Register. It also sets the first word and first byte latches and sets the GP reg bits to the Last Word, Flag, and End Regs as well as modifying the initial count and initiating the hardware controlled Selector Channel - I/O control unit sequences.

The channels logic circuits perform the Selector Channel - I/O control unit portions of the I/O operation on the interface independent of ROS control. The Unit Select routine called for by the Start I/O CCW-2 ROS routine sets up the interface linkages with the control unit of the selected I/O device. The diagram of Fig. 4-10 depicts the hardware controlled operations of the Unit Select Routine.

Once the CCW-2 routine requests the hardware to take over, ROS is no longer required to sustain the operation ROS takes a break-out cycle and returns to the CPU mode. It should be remembered that the CPU ROS was in a count-down loop and consequently will return to this loop. When the hardware routine has completed its work and ascertained the status of the I/O device, it will set the required stat 3 to cause the IOCE to break out of the count-down loop and continue processing this instruction. As indicated, this results in a stat 3 response and condition code being sent to the CE. The IOCE completes its operation then returns to the wait loop to await another instruction or an I/O break-in when the channel requires a data service.

The CE, upon receiving the condition code and stat 3 from the IOCE is now freed from its count-down loop and will return to I-Fetch for the next program instruction.

As indicated on the hardware Unit Select Routine flowchart, the selected I/O device will raise "Service In" to the channel hardware circuits to begin the

interface data sequence. This sequence will start the Tag Generator and store the byte on the bus in the C Register at the byte position designated by the Byte Counter (A section). This action will continue until the byte counter indicates that the C Register is full. When this register is full, the word is transferred to the B Register and Common Channel is requested to supply a Read-Store ROS routine. (This is the first I/O mode break-in since the IOCE ROS returned to the halt or wait loop.) This Read Store Routine updates the storage data address and stores the word from the B Register. It also updates the count field from the CCW and tests the End-Of-Record latches. If these latches are not set (which they would not be on the specified instruction) the ROS returns to the halt loop via a break-out routine and the reloading of the C Register is once again under hardware control. This sequence of loading the C Register under hardware control and requesting ROS routines to store the data in storage will continue until the last byte of data as specified by the count field of the CCW is transferred. At this time, the Read Store Routine will test the Chain Data Flag and if not set, will request the End Update Routine of ROS. The End Update results in the correction of the command address and the count in Local Store and the interrupt request being made. This interrupt request is gated through channel logic circuitry and, if the CE PSW bit is masked to allow, results in the CE taking an I/O interrupt.

As a result of the interrupt request from the IOCE, the CE will begin processing the interrupt at the end of the instruction it is executing. In processing this interrupt the CE will load the Preferential Storage Base Address on the External Bus to the IOCE and raise a tag line to permit the interrupt. The CE will then go into a count-down loop to await the IOCE response.

While the CE is in this count-down loop, the IOCE will, using its internal ROS routine, break from the halt loop and request the Interrupt Routine from Common Channel. While the IOCE is waiting on Common Channel to honor its request, it also goes into a count-down loop. The I/O mode operation of the Interrupt Routine in the Selector Channel causes the Channel Status Word

information to be loaded into the L, M, and R Registers. This data is then stored by CPU Mode Operation in the SE at the address specified by the PSBA + 64 (dec). The Unit Address is loaded into storage as the interrupt code. The IOCE then sends a response (stat 3) to the CE and returns to the halt loop. Upon receiving the (stat 3) reply from the IOCE the CE will branch out of the count-down loop and proceed to store the remainder of the PSW in the old PSW area. The new PSW is then loaded into the PSW Registers and becomes the current PSW, processing continues at the address specified by the IA portion of this control word.

While it is recognized that the foregoing discussion on the Selector Channel was greatly simplified, the scope of this course prevents discussion to greater depth. Additional information regarding this subject may be found in the following manuals:

1.	Input/Output Control Element Instruction Manual	CAB020
2.	Input/Output Control Element Panel Manual	CAB021
3.	System 360 Model 50 Selector Channel Theory of Operation Manual	CAA021-1
4.	7231-02 IOCE Diagram Manual	CAB520
5.	7231-02 IOCE ALD Manuals Vol. 1 - Vol. 21	CAB121-1 - CAB121-21

4-6. IOCE MULTIPLEXOR CHANNEL

The Multiplexor Channel is capable of servicing several I/O devices simultaneously when operating in the byte or multiplex mode. Actually, the channel is capable of servicing several devices sequentially (on a priority basis) and sustaining their operations simultaneously. The channel however is capable of sustaining only one operation at a time when operating in burst mode. The IOCE data flowchart of Fig. 4-15 indicates that the only additional functional units over and above those previously discussed are the Buffer 1, Buffer 2, and Buffer Latches.

The multiplexor handles data on a byte basis and as such requires the buffering provided by the 2 buffers and the associated latches. Both of the buffers are capable of accepting data from either the Mover or the Bus In from the interface. Both of the buffers are likewise capable of supplying data to the input to the Mover; however, only buffer 2 is capable of setting the Bus Out Latches to the interface. Figure 4-7 is the ILD for the buffer registers and the buffer latches while Fig. 4-8 is the logic flow for the Multiplexor Channel.

Operation on the Multiplexor Channel may be carried on in either byte mode or burst mode and may change modes in the same operation. When in burst mode, the I/O unit performing the operation remains logically connected to the interface. This differs from the byte (multiplex) mode in that in the byte mode the I/O unit is logically connected only during the time required to complete a data byte transfer. The channel facilities are time shared between the I/O devices.

The Multiplexor Channel is primarily ROS controlled in its operation. While the selector was controlled by sequential logic circuits (hardware), it had 12 ROS routines to accomplish the requested tasks. The Multiplexor on the other hand, has 34 ROS routines which are used to control its entire operation. The selection of these routines is a function of the Common Channel Circuitry and the Routine Request Generator. The channel receives its requests from the I/O devices (which are operating asynchronously). Channel in turn requests the appropriate ROS routine to service the request it received from the device. The channel request for ROS routine is serviced by the Common Channel which assigns a priority to it and in turn causes the Routine Request Generator to generate the starting address of the requested routine (when its turn comes up in the sequence). It is in this manner that the Multiplex Channel is capable of sustaining multiple operations.

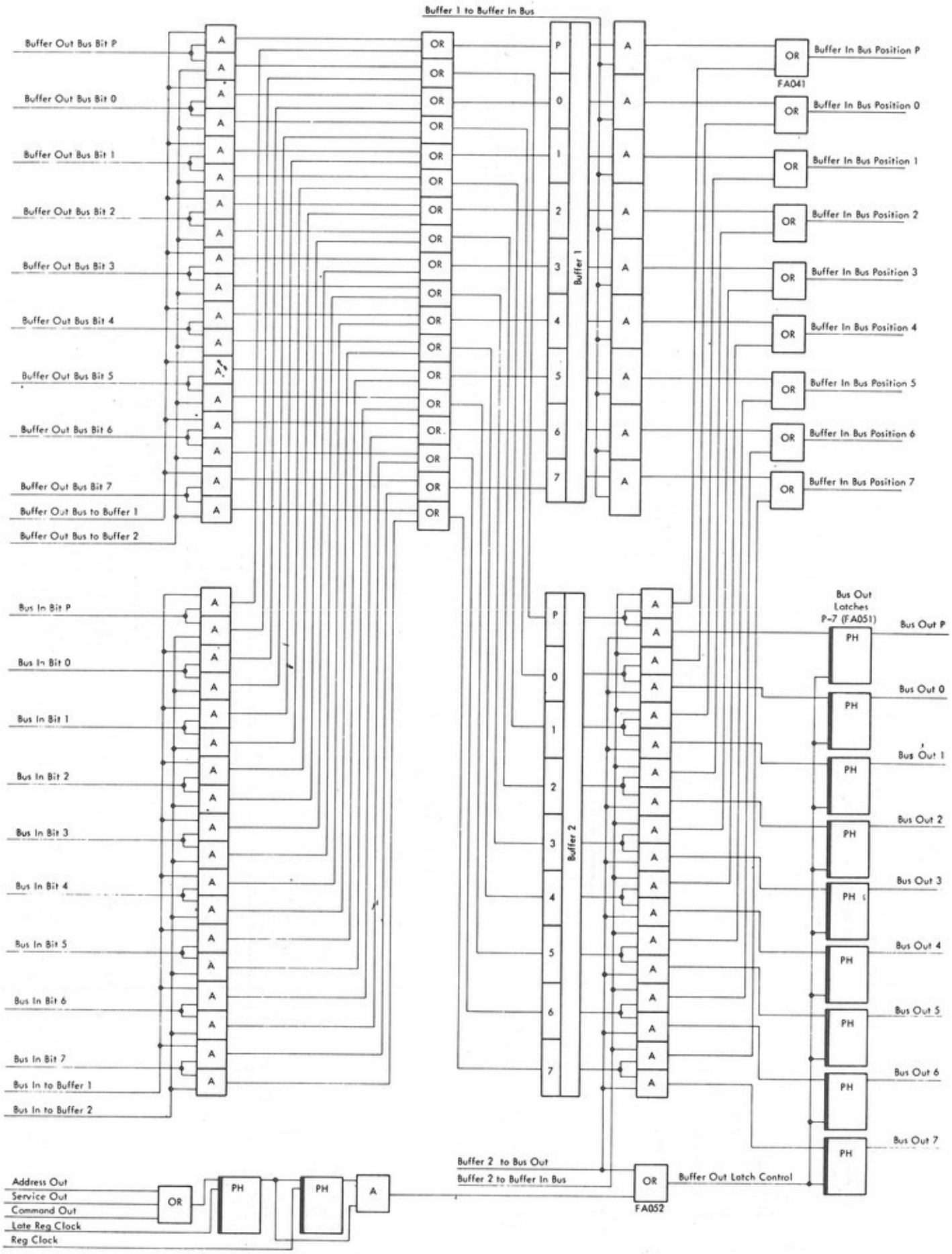


Figure 4-7. Buffer 1 and Buffer 2 Sets and Resets.

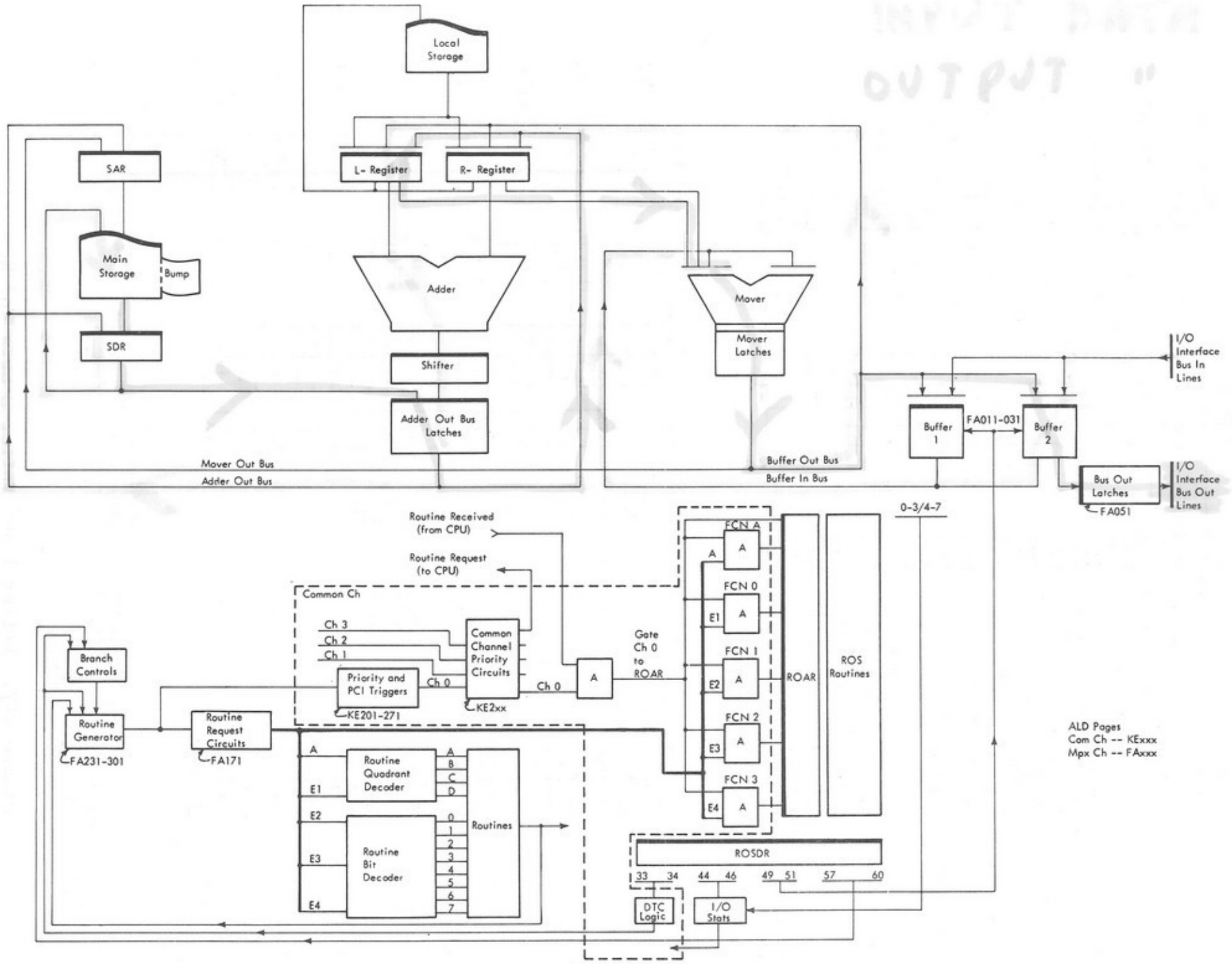


Figure 4-8. Data Flow in Multiplexor Channel Operations.

The 34 ROS routines which the Multiplex Channel has available for its operational control are all executed in the I/O mode, and as such, require that a break-in take place. At the end of each of the routines, Common Channel tests its priority control circuits to ascertain if a routine with a higher priority has been requested. Assuming that none has been, the Routine Request Generator will start into the next lowest priority routine or permit the continuation of the sequence. If there are no routine requests pending (higher or lower priority) the IOCE ROS will perform a break-out cycle and return to CPU mode. The 34 routines are functionally divided into 5 general categories.

"A" type routines which in general deal with the CCW and data handling include:

- AØ - Count Fetch and Update
- A1 - Data Address Fetch and Update
- A2 - Data Address and Count Correction
- A3 - Data Handling
- A4 - End Status Analysis
- A5 - Comm Chain End Status Analysis
- A6 - Interrupt Preparation
- A7 - Count = Ø Analysis

The "B" type routines deal primarily with the SIO instruction and the interface operation during this instruction. Routines B5 and B6 are multipurpose routines and may be used with other categories.

- BØ - Sequence Control Fetch
- B1 - Start I/O Unit Select
- B2 - Start I/O Unit Address Compare
- B3 - Status Analysis
- B4 - Unused
- B5 - Count Store
- B6 - Data Address Store
- B7 - Channel Check Handling

The "C" type routines in general deal with the interface operation for the other program instructions which the channel is capable of performing.

- CØ - PCI
- C1 - Test I/O Unit Select - 1
- C2 - Test I/O Unit Address Compare
- C3 - Test I/O Accept Status
- C4 - Control Check
- C5 - Control Unit Busy
- C6 - HIO Unit Select
- C7 - Test I/O Unit Select - 2

The "D" routines in general deal with the chaining operations specified in the CCW for the operation being performed. Since in the original I/O instruction processing CCW word 1 was fetch and processed in CPU mode, provisions had to be made to permit fetching the additional CCW-1 words in chaining operations.

- DØ - Command Address Fetch/Store
- D1 - CCW-1
- D2 - Command Chain - UA Compare
- D3 - Command Chain - Initial Status Analysis
- D4 - CCW-2 Fetch
- D5 - Load 64 Prep-Test I/O No End Qued
- D6 - Not Used
- D7 - Data Chain

The interrupts are handled under the control of the "H" routines.

- HØ - SPCI Interrupt
- H1 - Interrupt Handling
- H2 - Interrupt Handling - 2
- H3 - Interrupt Handling - 3

The flowchart of Fig. 4-19 is the general routine selection sequence for typical I/O operations on the Multiplex Channel. Figure 4-9 is the flowchart for a typical routine.

The general routine selection sequence chart is not in the true sense of the words a flowchart since there is no differentiation made between the hardware operations and those of the ROS routines. This chart is presented merely to acquaint the student with the normal sequencing of the routines. For a more complete analysis of the Multiplexor Channel ROS routine selection the student is advised to consult the flow diagrams in FAA manual CAD-520.

Figure 4-9 is the logic flowchart of the B1 Unit Select ROS routine. The decisions made in this routine are made as a result of the A and B branch bits of ROAR. These bits would be set as a result of channel action on the I/O stats, or as a result of the data supplied to the beginning u-instruction. This figure also indicates that there are exits from this routine to hardware sequential logic circuits.

These circuits would set the stat 3 reply, and set the condition code to 2. Setting the stat 3 reply would allow the IOCE to exit from its count-down loop, this in turn would cause the response to be sent to the CE. The condition code being set to 2 would present a Unit Busy Status to the CE as a result of the I/O instruction.

Note that the operation of the Multiplex SIO is identical to the SIO on the Selector Channel (as shown on Fig. 4-17) until the IOCE goes to the count-down loop. The operation is identical when the stat 3 reply is received. The only difference between the two types of channels is in the I/O mode operations while in the initial selection, and the manner in which data is transferred to storage and to the device.

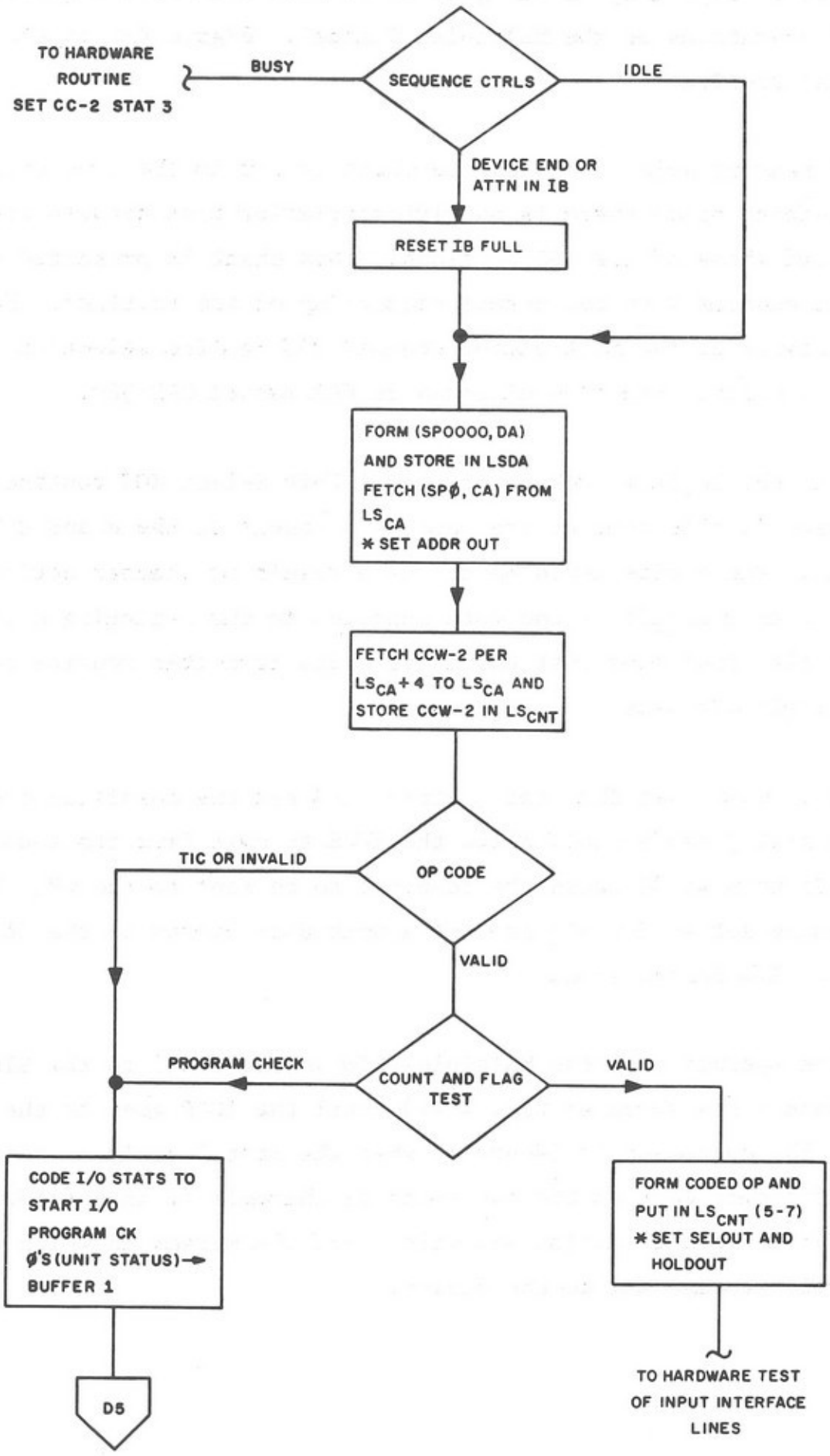


FIGURE 4-9 MULTIPLEXOR BI ROUTINE

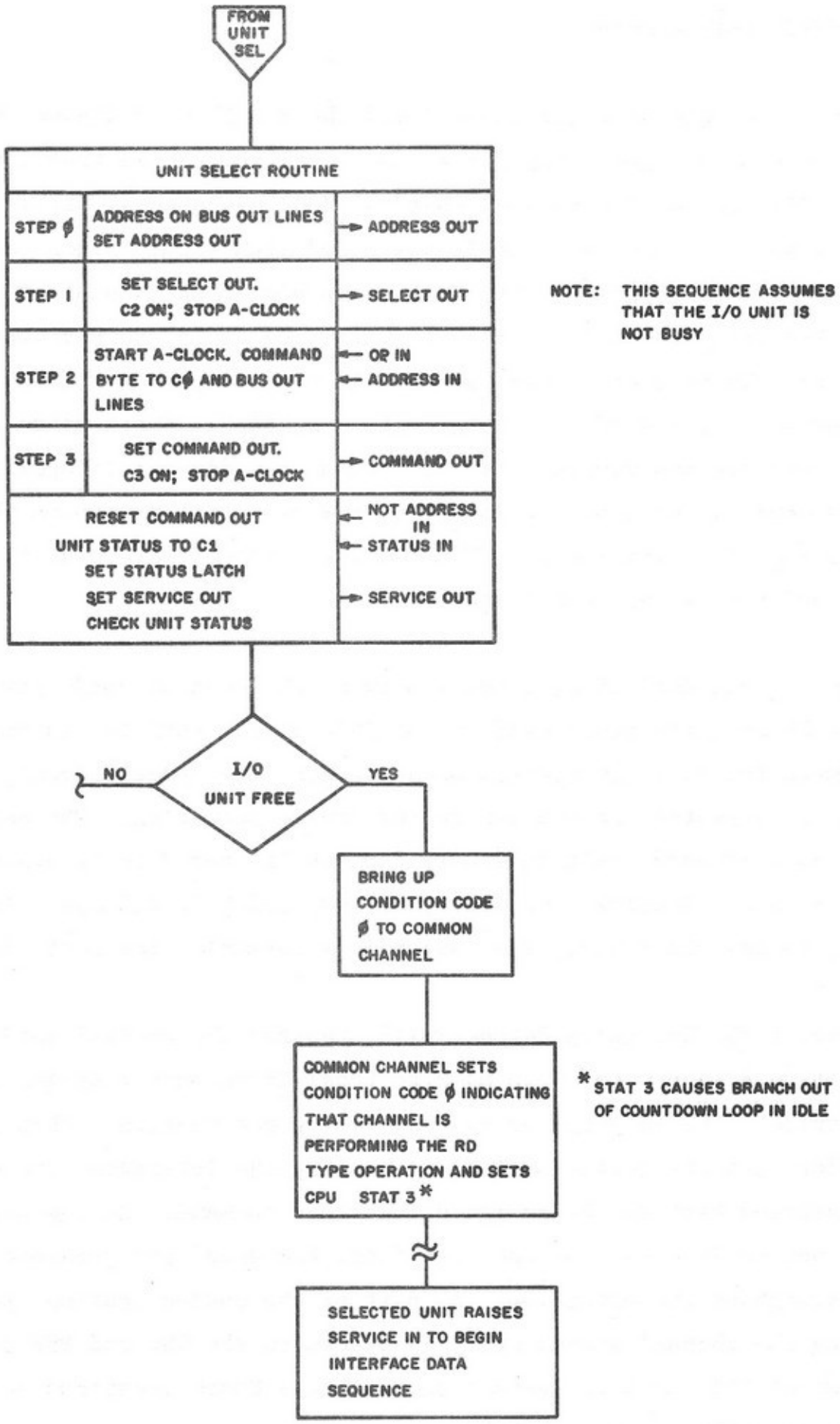


FIGURE 4-10 SELECTOR CHANNEL HARDWARE UNIT SELECT ROUTINE

4-7. UNIT CONTROL WORDS

Up to this time the Selector Channel and the Multiplexor Channel have been treated as separate and independent functional units. In truth, these functional units are so interrelated that the IOCE has special provisions to literally keep track of what it is doing and with whom. Since there are two Selector Channels (possibly three) each capable of sustaining an I/O operation and one Multiplex Channel capable of sustaining up to 256 simultaneous I/O operations, the problem becomes acute. In practice, each Selector Channel is allocated 4 control words to sustain its operation. These words are contained in Local Storage and remain there as long as the channel is operating with the selected device. Each of the possible devices on the Multiplex Channel are assigned 4 control words also. These words, however, are stored in MACH storage and are brought out as required.

There is a great deal of similarity between the control words used for the Selector Channel and those used on the Multiplex. Both for instance contain the Command Address, the updated Data Address, the updated Count, and other information essential to sustaining the device operation. The Selector Channel control words omit information which is stored in hardware registers such as Sequence Controls, Op Codes, Status, and Unit Address. The Multiplex Channel, on the other hand, will use this information for control.

In operation the Multiplex Channel will transfer the control words (UCW) from the location assigned to it in MACH to Local Store when a device requires a data service. The information is used during the routine. When the routine is complete and the device no longer is using the interface, the updated data is transferred back to its assigned locations in MACH. On the Selector Channel the device is always on the interface, the words are retained in Local Store throughout the operation. As part of the ending routine, pertinent data regarding the channel status etc., is placed in the CSW and PSW area of the SE. Some of this data is taken from the Local Store locations and some of it is taken from the hardware latches.

Figure 4-11 is the Local Store map for the IOCE. Notice that provisions have been made for the optional third channel even though this channel may not be installed. Notice also that there is only one group of registers set aside for the Multiplex Channel. This, as was explained previously, is due to the fact that only one device at a time may utilize the channels facilities.

Figure 4-12 is the format of the control words in the MACH Store locations. These words occupy an area of MACH referred to as "BUMP" store, and are unique to the Multiplex Channel. Actually, "BUMP" store is the high order 1024 words of MACH. (4 words x 256 devices) These control words referred to as the UCW will contain the data indicated and present a method whereby the channel can ascertain the previous ending conditions of a device. As a matter of convenience to the microprogrammer the indicated data may be modified by certain routines, however, in the ending analysis the data will be presented as indicated.

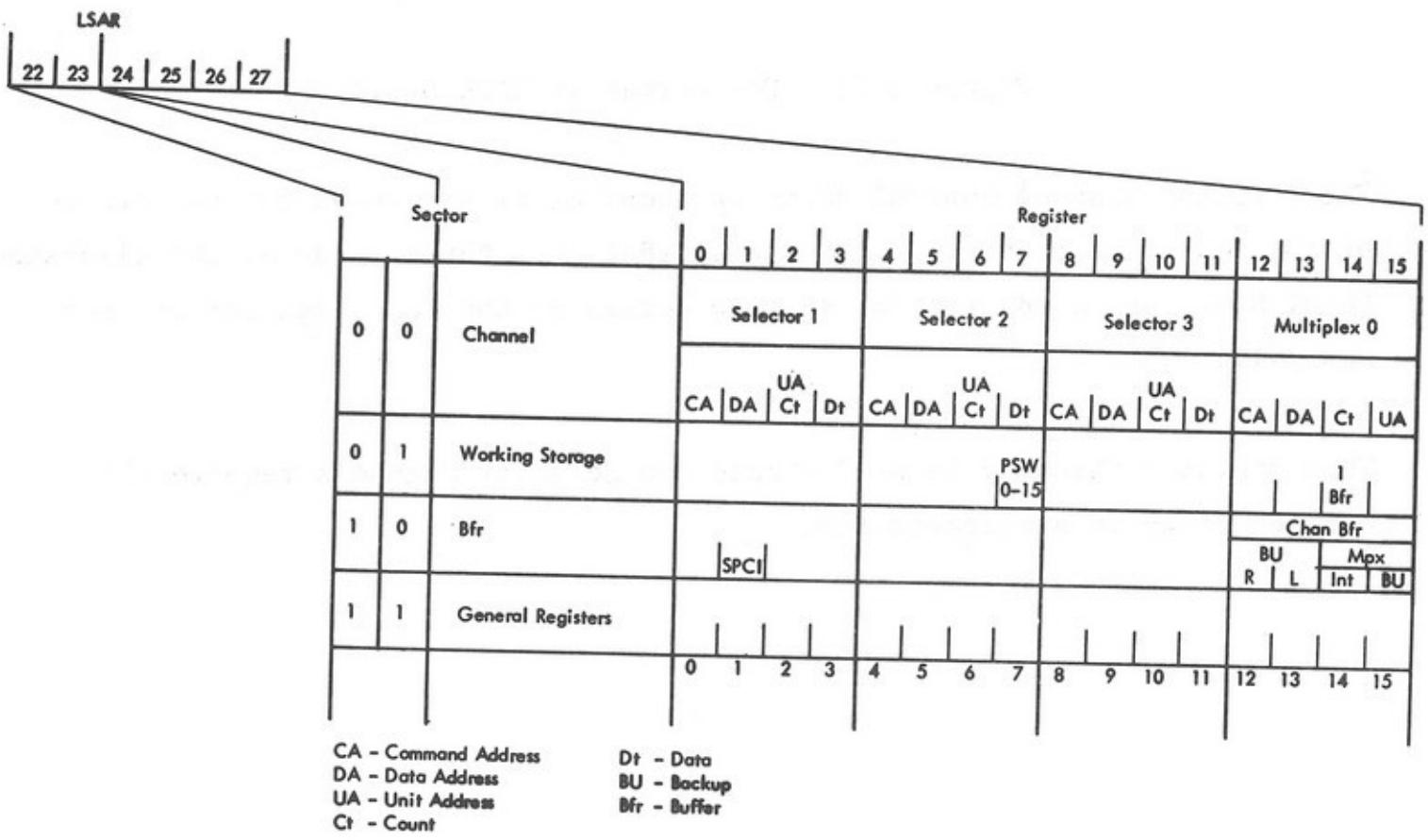


Figure 4-11. Local Store Map for IOCE.

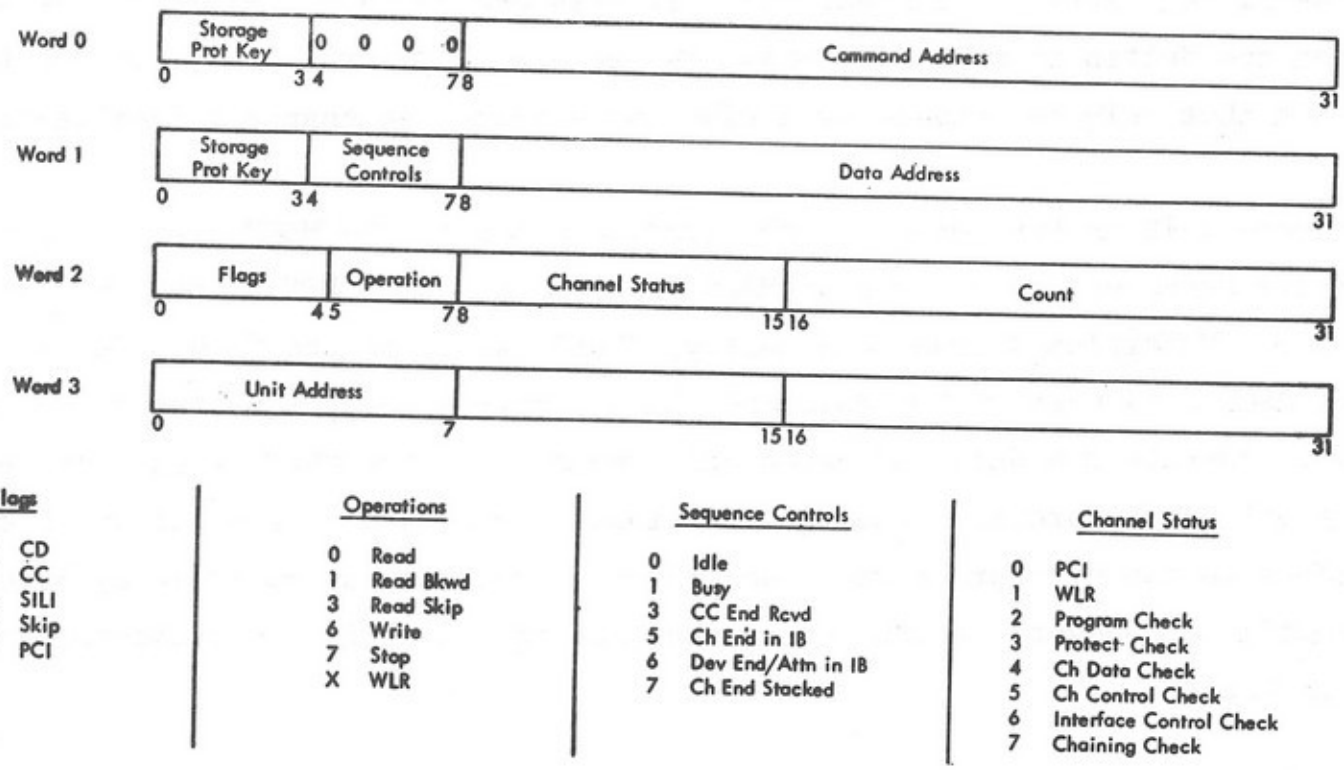


Figure 4-12. UCW Format in MACH Store.

MULTIPLEX

The Selector Channel control words in Local Store are shown for two stages of the operation in Fig. 4-13. Notice that only three words of the allocated Local Store are used, the fourth word serves as the data register for the channel.

This register then may be used should two Selector Channels require the service of an SE simultaneously.

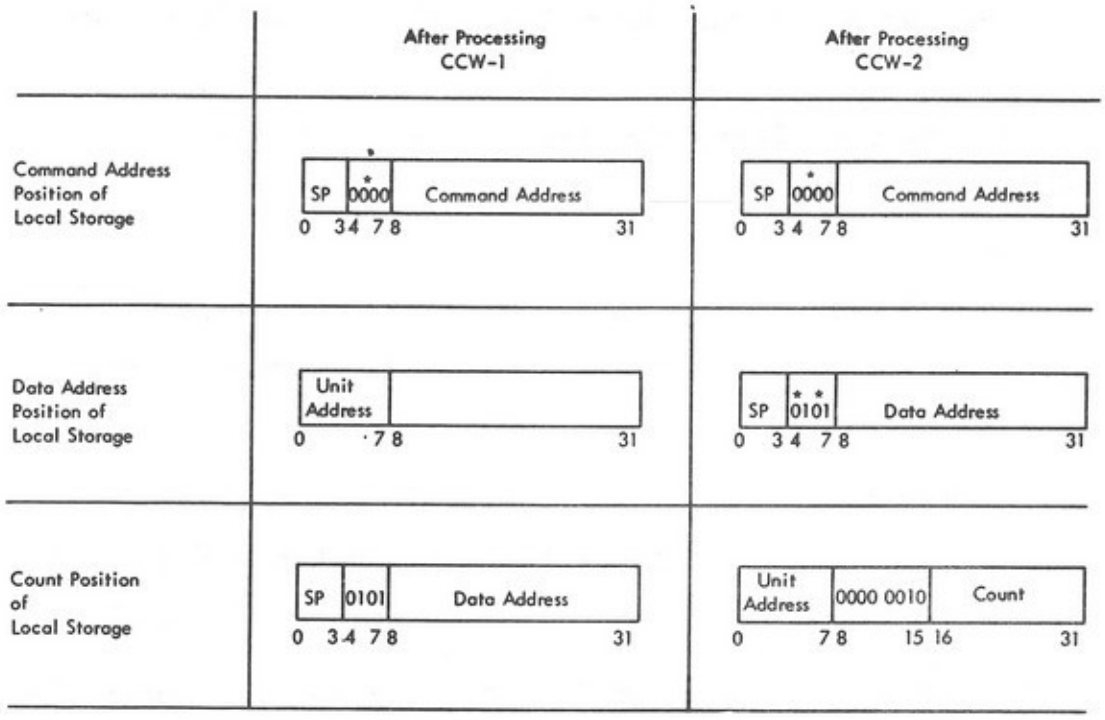


Figure 4-13. Selector Channel Local Store Positions.

4-8. IOCE STANDARD INTERFACE

Data transfers and controls between the IOCE and the external devices are accomplished on a Standard Interface Cable. The block diagram of the standard interface is shown in Fig. 4-14. This connection between the IOCE channels and the I/O control unit provides an information format and a signal sequence common to all control units. The interface consists of a set of 34 lines that connect a number of control units to a channel. Except for signals used to establish selection control, all communications to and from the channel occur over a common bus, i.e., any signal provided by the channel is available to all control units. At any one instant, however, only one control can logically be connected to the channel. Selection of a control unit for communication with the channel is controlled by a signal passing serially through all control units that permits, sequentially, each control unit to respond to the signals provided by the channel. A control unit remains

logically connected on the interface until it transfers the information it needs or has, or until the channel signals it to disconnect.

For purposes of simplicity the I/O interface is divided into five functional categories:

(1) BUS OUT - Used to transmit information (data, I/O device address, commands, control orders) from the channel to the control unit.

(2) BUS IN - Used to transmit information (data, I/O device identification, status information, sense data) from the control unit to the channel.

(3) TAGS - Used for interlocking and controlling information on the buses and for special sequences.

(4) SEL CTRLS - Used for the scanning of, or the selection of attached I/O devices.

(5) METERING - Used for conditioning of elapsed time meters in the various attached units.

A. BUS Information

Each of the buses (in and out) consists of eight information lines and one parity line. Information on the buses is always arranged so that bit position 7 always carries the low order information bits and the bits proceed from right to left, thus any unused information lines will appear in the high order positions (0, 1, 2.....etc.). The information transmitted over the bus is indicated by the appropriate tag line, i.e. when "Address Out" tag is active, the bus out will contain valid address information; when the tag "Status In" is active, the bus in will contain a byte of information describing the status of the I/O device.

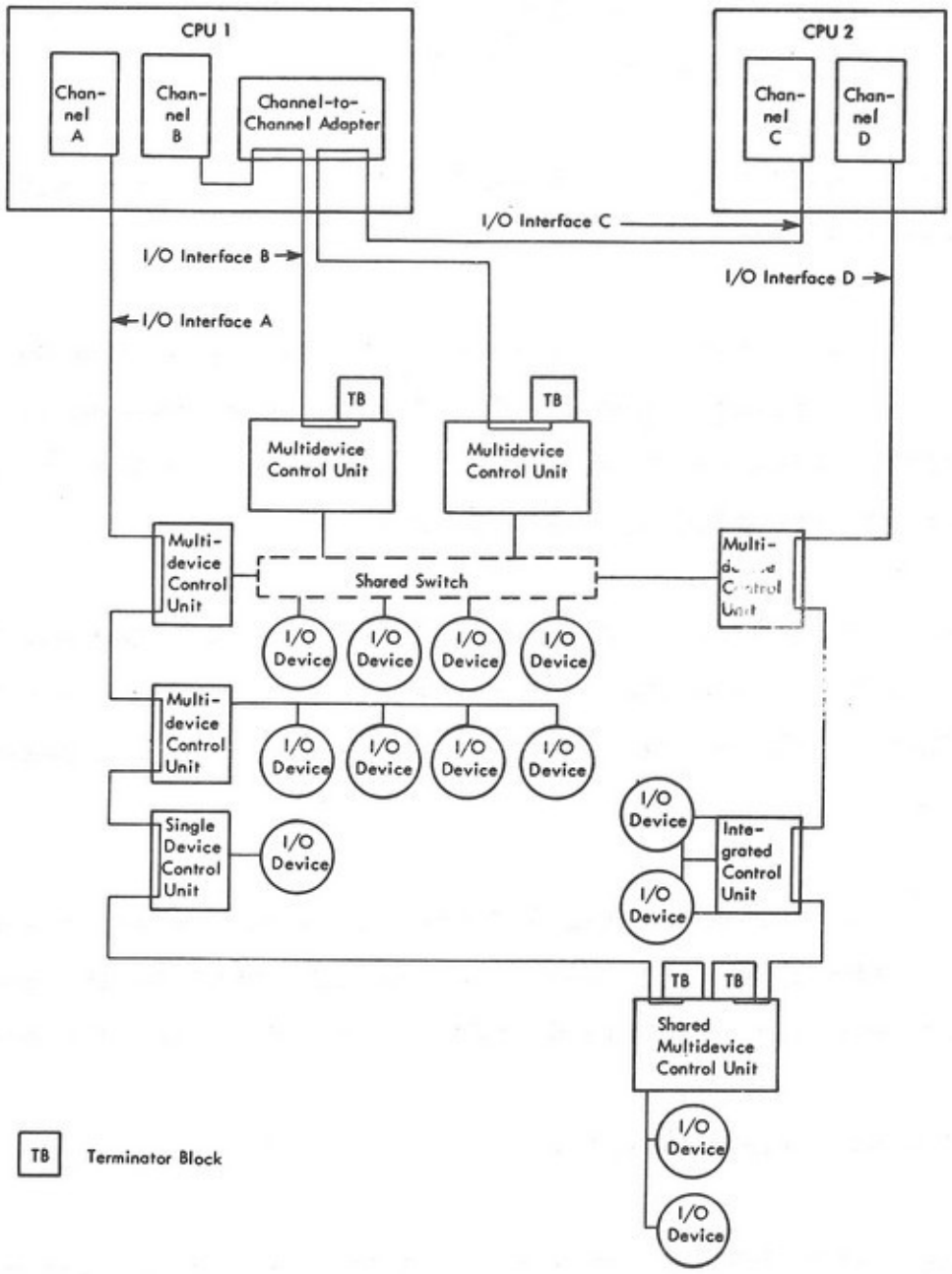


Figure 4-14. Input/Output Interface—Multiple Configurations.

B. Interface Tag Lines

Address-Out: Active during the channel initial selection sequence, bus-out specifies the address of an I/O device.

Command-Out: Active during channel initial selection sequence when the bus-out specifies a command.

Service-Out: Is active in response to a service-in tag during the execution of a Write or Control Command. The data on the bus-out is dependent upon the operation being performed, for instance on a Write the bus will contain the data to be recorded by the I/O device.

Address-In: Is active as a result of channel tag "Address Out" the bus-in at this time will contain the address of the selected I/O device. When this tag line is active, the bus-in contains the address of the currently selected I/O device.

Service-In: Is active during the execution of a read or sense command. The data on the bus-in will depend upon the instruction, for instance on a read command the bus will contain a byte of data from the I/O device.

C. Selection Control Lines

Operational-Out: Used as an interlock to all control units. With the exception of the suppress-out line, all lines from the channel are significant only when the operational-out line is active.

Operational-In: Is a line from all attached control units used to signal channel that an I/O device has been selected, and is communicating with the channel.

Select-Out: Is a line propogated from the channel to the highest priority I/O control unit, and thence from this control unit to the next lower priority unit. This line provides a loop for scanning the attached control units. The Select-Out line returns to the channel as a Select-In line.

Select-In: This line emanates from the lowest priority control unit and provides the return path for the Select-Out line to the channel.

Suppress-Out: Is a line from the channel to the control units and is used both alone and in conjunction with the out-tag to provide the following special functions: Suppress Data, Suppress Status, Command Chaining and Selective Reset.

Request-In: Is a line from all attached control units to the channel. This line is used to signal channel when any control unit has a data service or status service requirement.

D. Metering Control Lines

Metering-Out: Is a line from the channel to the I/O control unit used to condition all attached control unit and device elapsed time meters to run.

Metering-In: Is a line from all attached control units to the channel which permits the system elapsed time indicator to run even though the system may be in the stopped or wait state.

Clock-Out: Is a line from the channel used to indicate that the processor is not stopped or waiting.

Since the 9020 System does not have an elapsed time meter, the metering control lines and clock-out lines are not utilized. Elapsed time meters on the Tape Control Unit, and the 2821 Integrated Control Unit must however be enabled for these units to function.

4-9. IOCE STAND ALONE OPERATION

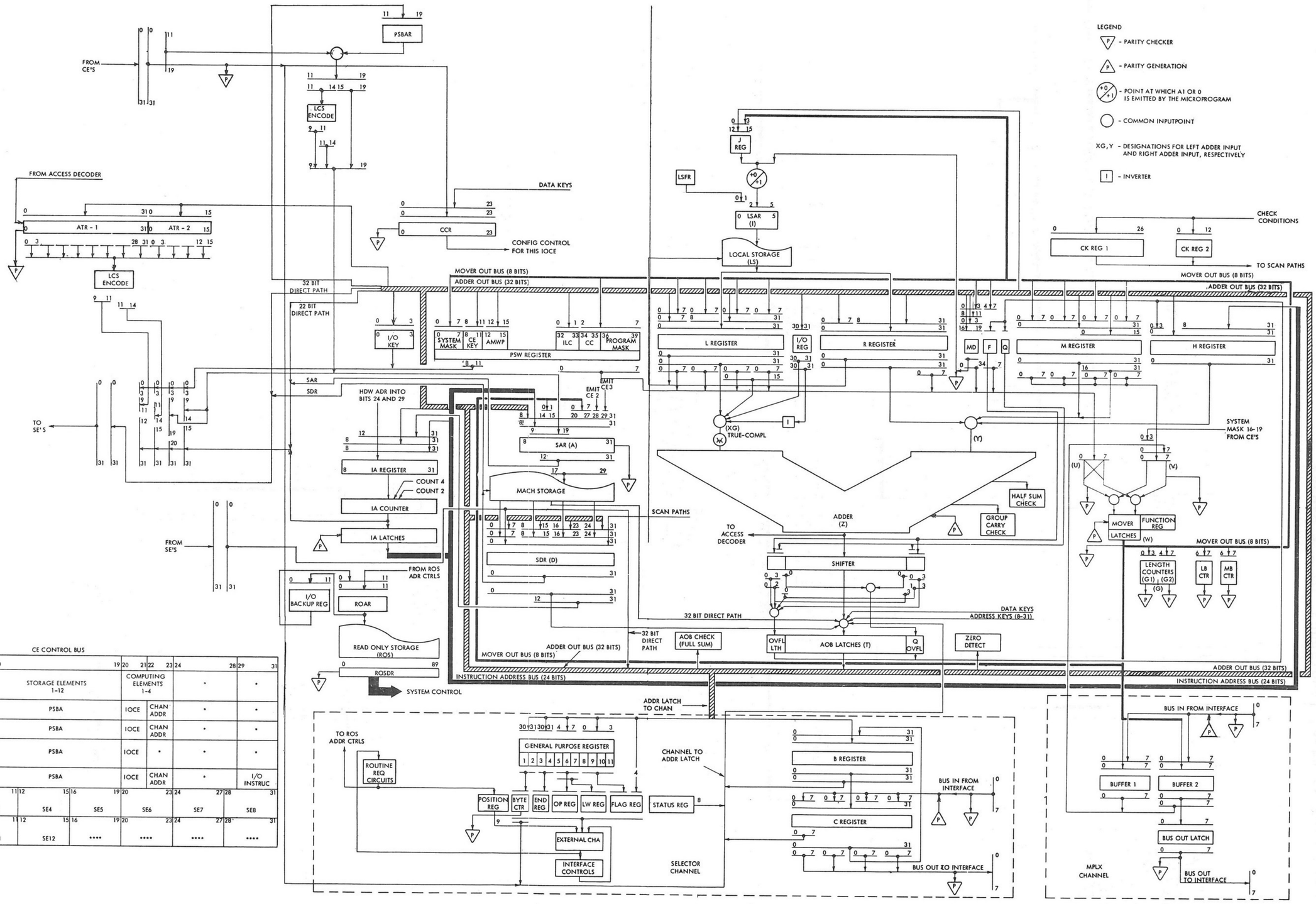
To facilitate the maintenance of the 9020 System each of the elements associated with the system are capable of certain manual operations. These operations are normally limited in their scope since no single element up to this time contains all of the essential logic circuitry. The IOCE however contains all of the facilities to perform as a standalone computer. The IOCE contains its own internal control (ROS), it contains its own common logic unit for processing data (CLU), it contains its own storage capability (8K MACH), and it contains logic to permit communication with the external environment (Channel - I/O, and I/O - Channel).

To make use of this unique feature of the IOCE it is necessary that the IOCE be placed in the "Diagnostic" mode. (Any time there is no CE bit on in the IOCE Configuration Control Register the IOCE is in the Diagnostic Mode.) If it is desired to further isolate the IOCE from the operating system, the test switch may be turned on (down).

When operating in the diagnostic mode the IOCE closely resembles the operation of the IBM System 360/Model 50. That is, it is capable of performing Initial Program Loads, (IPL) executing the standard Model 50 instruction set (no Floating Point or Decimal features), and processing the normal interrupts. It should be borne in mind however that the size of the programs is limited by the 8K of available storage. This storage is not all available to the program since the upper 1024 words are utilized as channel UCW area, and the lower 256 bytes are designated for PSW's, CAW, CSW, and the Diagnostic Scan-out area.

The diagnostic standalone capabilities of the IOCE are primarily intended for use in element maintenance programs such as the Fault Locating Tests and the Sub-System Diagnostic Monitor. This does not preclude the possibility of utilizing this feature for running the Diagnostic Sections used for testing the Various I/O devices, nor for the execution of small scale programs. As previously mentioned the size of these programs is limited by the storage available.

The ability to use the IOCE as a standalone processor permits the technician or engineer to use this element to "bootstrap" the system up to operating capability. Since all of the maintenance programs require some form of input device, the technician or engineer may, with built-in tests and FLT's, verify the operation of the IOCE. Then using the pre-tested IOCE, and the SDM tests, he may verify the operation of the Storage Element. He may then, with a manually configured system use the IOCE and SE to load the FLT's for testing the CE. He may then use the FLT's to locate and correct any CE malfunctions. Having accomplished this the engineer or technician may run the MDM's and SEVA tests to assure the systems operation.



CE CONTROL BUS

	0	1	2 3 4 5	6	7	8 9 10 ... 19	20 21 22 23	24 ... 28	29 ... 31
CCR	OS 0	IS 1	SCON	A	*	STORAGE ELEMENTS 1-12	COMPUTING ELEMENTS 1-4	*	*
IPL	UNIT ADDRESS			*	*	PSBA	IOCE	CHAN ADDR	*	*
FLT	UNIT ADDRESS			*	*	PSBA	IOCE	CHAN ADDR	*	*
PERMIT IRPT & LOGOUT	*			*	*	PSBA	IOCE	*	*	*
INSTRUC	UNIT ADDRESS			*	*	PSBA	IOCE	CHAN ADDR	*	I/O INSTRUC
ATR SELECT WORD 1	0 3	4 7	8 11	12 15	16 19	20 23	24 27	28 31		
	SE1	SE2	SE3	SE4	SE5	SE6	SE7	SE8		
ATR SELECT WORD 2	0 3	4 7	8 11	12 15	16 19	20 23	24 27	28 31		
	SE9	SE10	SE11	SE12	....	....	....	....		

* - INDICATES UNUSED BITS
A - INDICATES INHIBIT LOGOUT STOP

Figure 4 - 15 IOCE Data Flow Registers

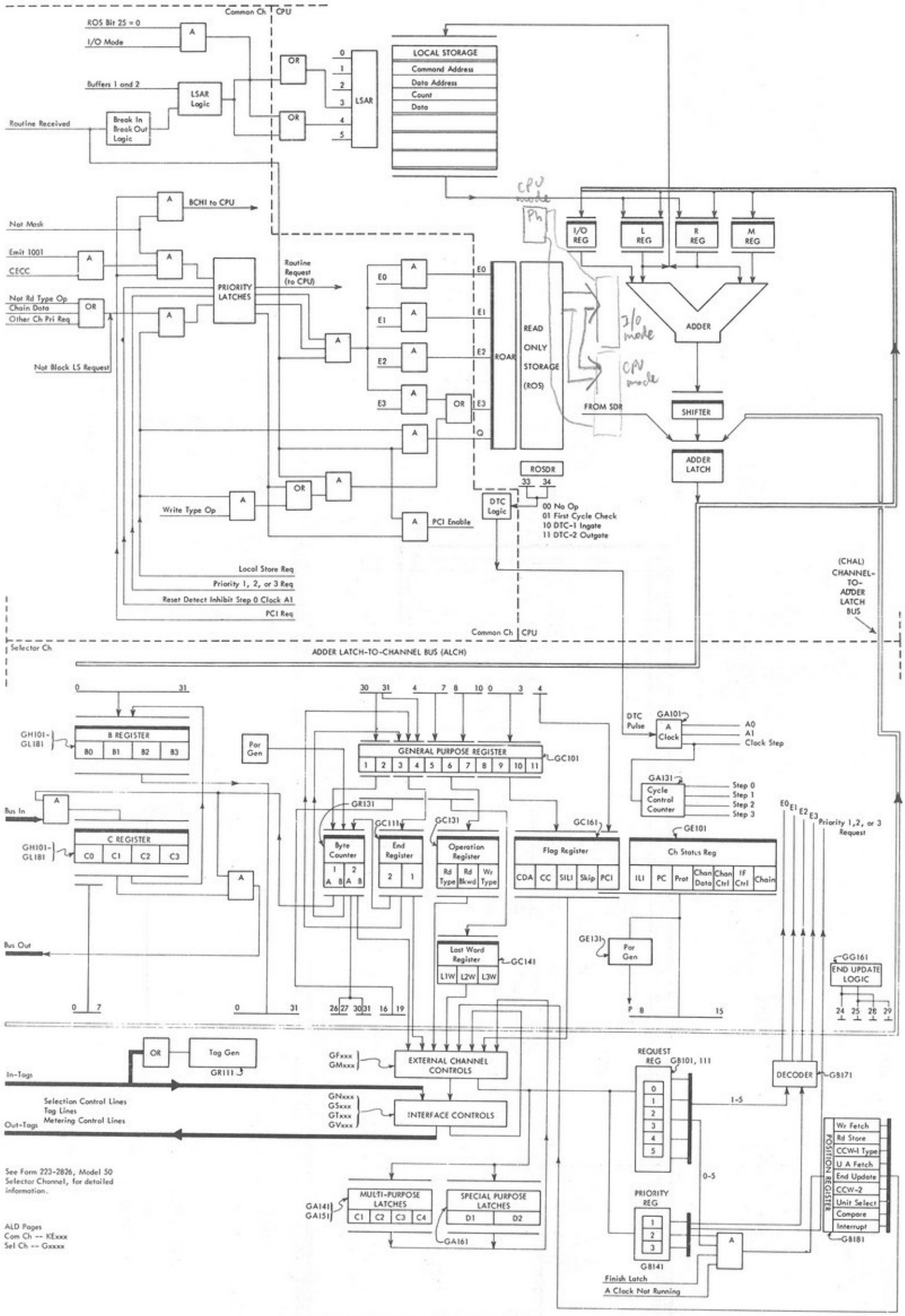


Figure 4 - 16 Functional Units of Selector Channel

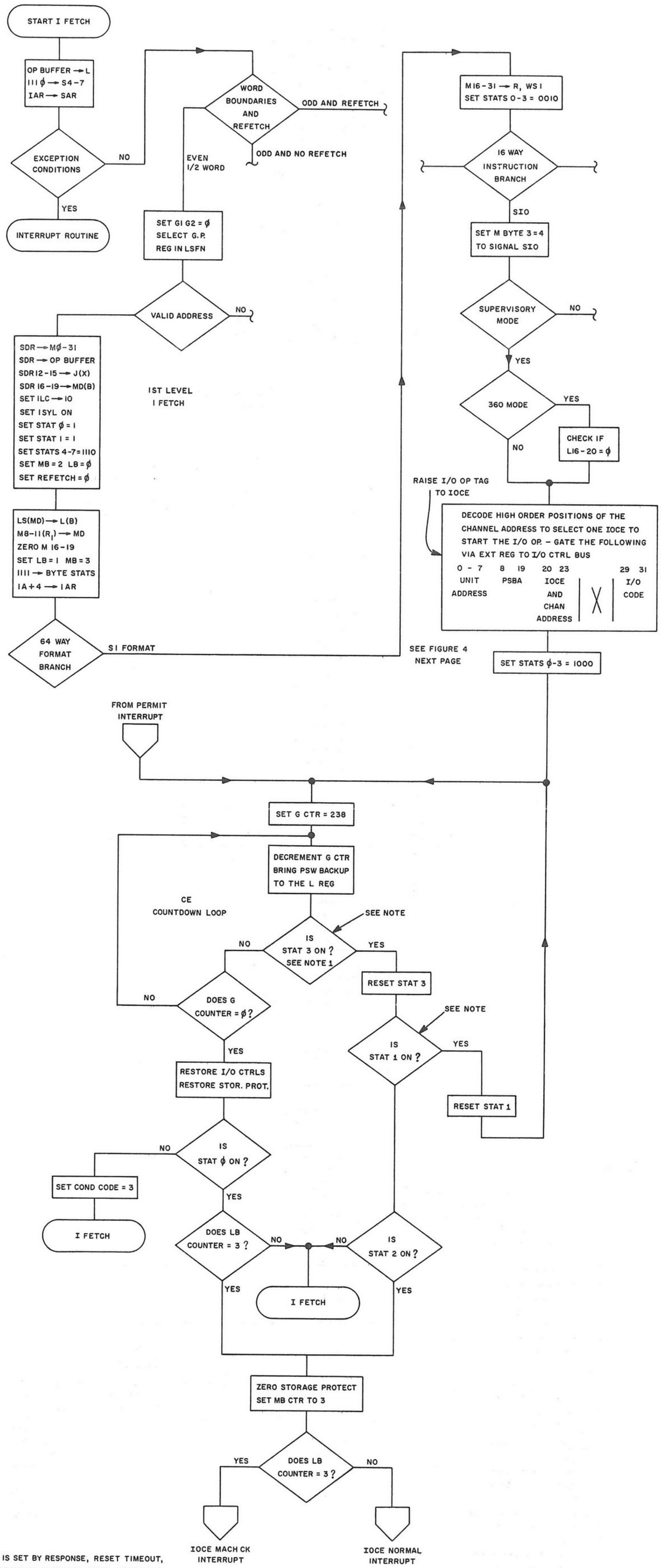


FIGURE 4-17 COMPUTE ELEMENT START I/O, INTERRUPT

NOTE:
STAT 3 IS SET BY RESPONSE, RESET TIMEOUT, PSBAR LOCKOUT, ELEMENT CHECK, OR MACH CK, IN THE LATTER 3 CASES CONDITION CODE 3 WILL ALSO BE SET BY HARDWARE.
STAT 1 WILL BE SET BY RESET TIMEOUT FROM THE SELECTED IOCE UNDER NORMAL CONDITIONS.
ELEMENT CK, PSBAR LOCKOUT, OR IOCE MACHINE CK, WILL BLOCK RESET TIMEOUT AND RESET STAT 2. (FOR IOCE NORMAL PERMIT INTERRUPT ONLY)

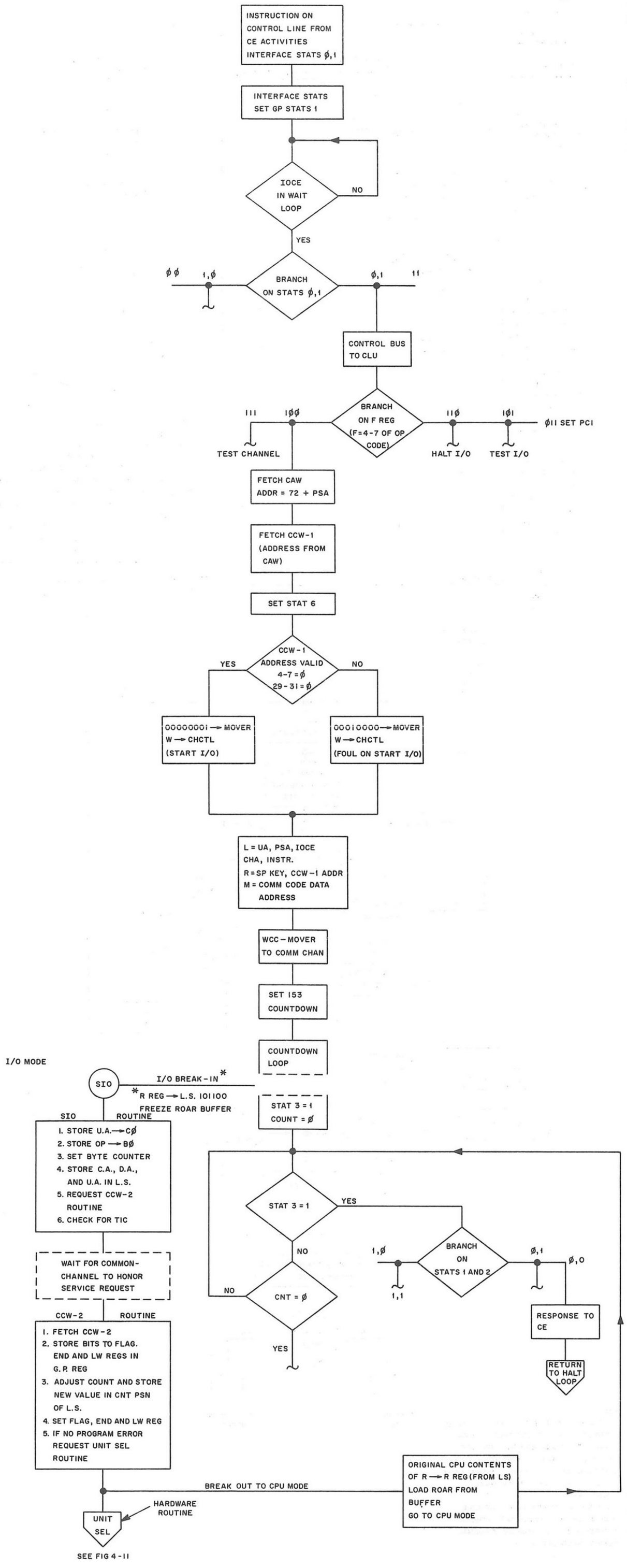


FIGURE 4-18 IOCE START I/O

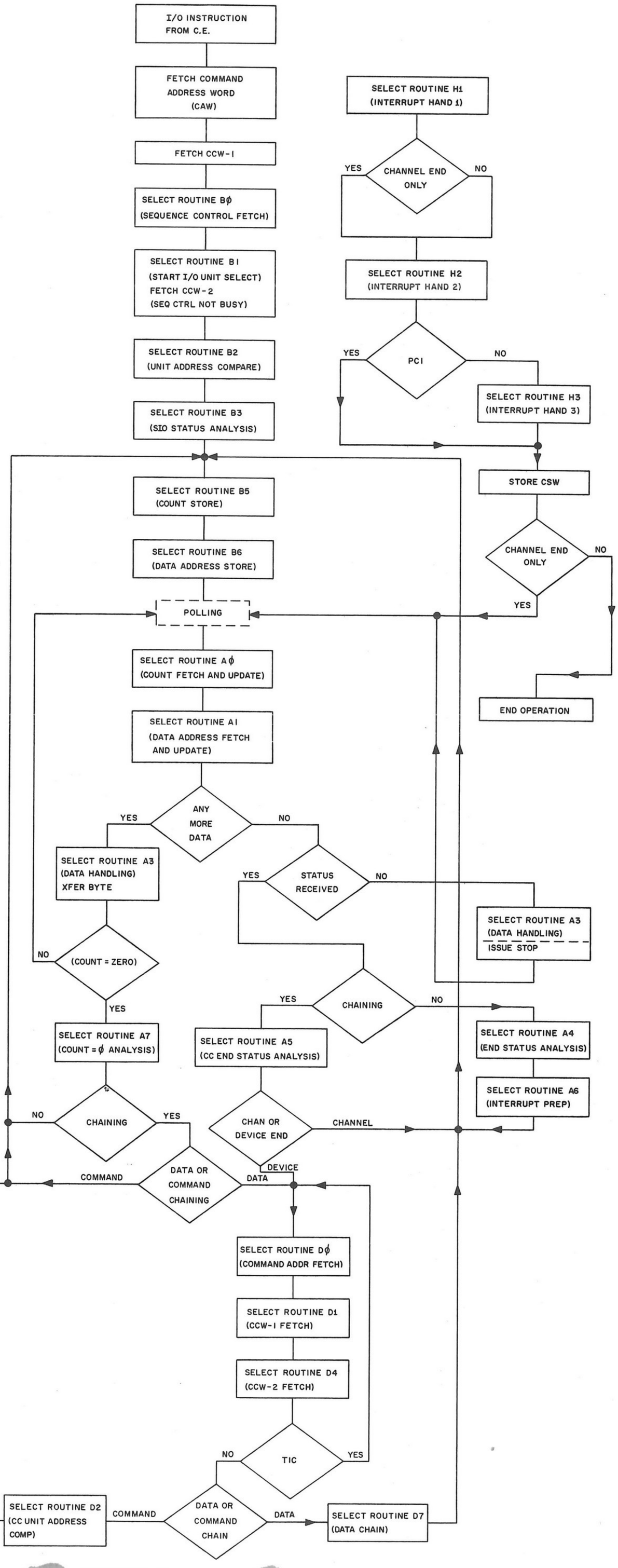


FIGURE 4-19 IOCE MULTIPLEX CHANNEL ROUTINE SELECTION SEQUENCE